

Introduction to CMOS VLSI Design

Design Flow

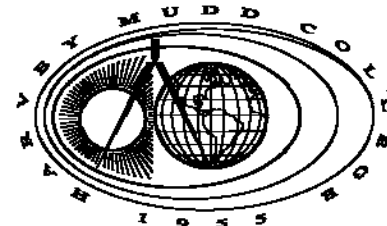
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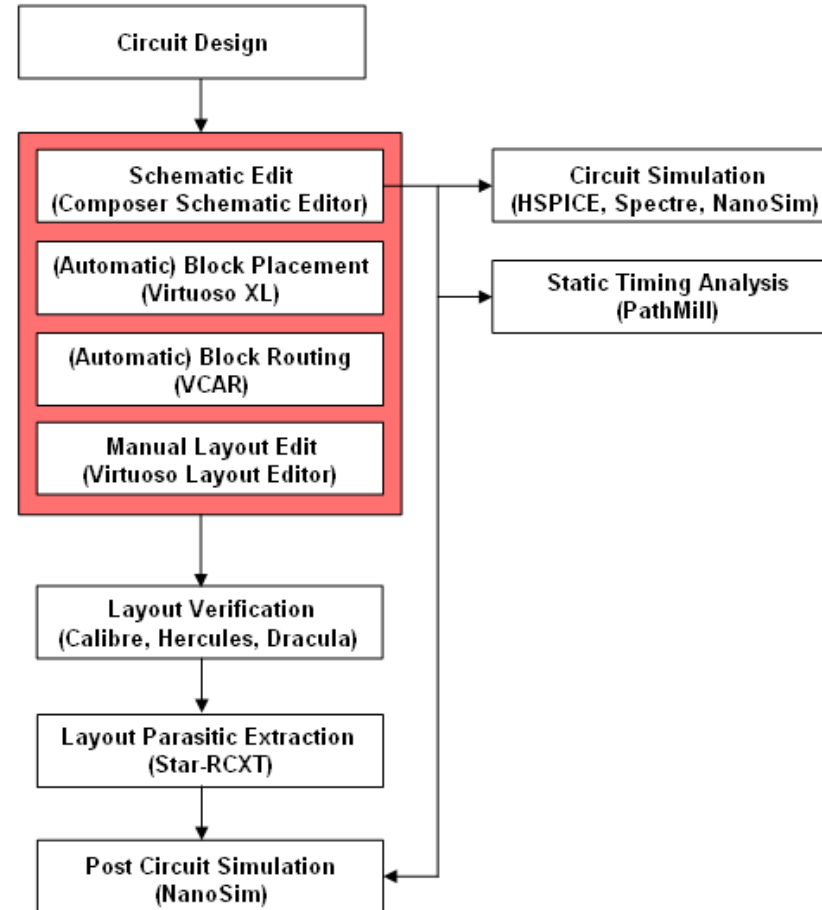
courtesy of David Harris (Harvey Mudd College)



Chungnam National University



Design Flow (Analog)





RTL Description

Verilog HDL

□ Verilog

- Verilog was invented by Phil Moorby and Prabhu Goel in 1983 at Automated Integrated Design Systems (later renamed to Gateway Design Automation in 1985)
- Gateway Design Automation was later purchased by Cadence Design Systems in 1990.
- Similar to C Language
- Currently dominates industries especially for hardware implementation

□ cf) Verilog-2001, Verilog-2005, SystemVerilog

VHDL

□ VHDL

- originally developed at the behest of the US Department of Defense in order to document the behavior of the ASICs that supplier companies were including in equipment.
- That is to say, VHDL was developed as an alternative to huge, complex manuals which were subject to implementation-specific details.
- Mostly from ADA(Programming Language)
- Similar to Pascal Language